AD-A052 367 STANFORD UNIV CALIF DIGITAL SYSTEMS LAB F/G 9/5

INITIAL DESIGN CONSIDERATIONS FOR A HIERARCHICAL IC DESIGN SYST--ETC(U)

NOV 77 W M VANCLEEMPUT, E A SLUTZ

UNCLASSIFIED DSL-TN-132 NL

| OF |

AD A052367

END

DATE FILMED

5-78

DDC

INITIAL DESIGN CONSIDERATIONS FOR A

HIERARCHICAL IC DESIGN SYSTEM

W. M. vanCleemput & E. A. Slutz

Technical Note No. 132

November 1977

Digital Systems Laboratory
Stanford Electronics Laboratories
Stanford University
Stanford, California 94305

This work was supported by the Joint Services Electronics Program under Contract N-00014-75-C-0601.

Digital Systems Laboratory
Stanford Electronics Laboratories

(10) W. M. vanCleemput ~~&~~ E. A. Slutz

(9) Technical Note No. 132 (14) DSL-TN-132

(11) Novem[redacted] 1977 (12) 30p.

(6) INITIAL DESIGN CONSIDERATIONS FOR A HIERARCHICAL IC DESIGN SYSTEM,

ABSTRACT

This paper describes the initial design of a comprehensive hierarchical integrated circuit design system, that is currently being implemented at Stanford University. This system encourages the use of structured hardware design techniques. It is intended for the design and layout of large-scale integrated circuits by means of a combination of manual and algorithmic techniques.

INDEX TERMS: integrated circuit design, hierarchical design system, design automation, LSI circuit layout

408 071

1. DESIGN PHILOSOPHY

This system is based on the premise that the process of designing any large scale system is hierarchical in nature. Some proponents of structured software design propose a top-down design strategy and a bottom-up implementation strategy. For very complex hardware systems a similar discipline may greatly improve the correctness of the design and the time required to obtain the solution. As we quickly approach the point where a ten-thousand or even a fifty-thousand-gate chip design becomes feasible, it becomes important to devise a design methodology that will allow both rapid and correct design of such circuits.

Typically, the logic design of a digital system is done in a top-down fashion, while the implementation is done in a bottom-up fashion mainly. In actual practice, however, both logic design and layout are done by means of a combination of top-down and bottom-up approaches. Therefore, a design system should be able to incorporate both strategies in order to allow the designer the flexibility he needs to obtain a satisfactory design. This hierarchical design strategy is very similar to the way in which the human designer attacks a large design problem.

Currently, integrated circuit design is supported by a collection of often loosely connected programs, such as logic simulators, automated placement and routing, circuit analysis and design rule verification. The use of automated layout methods depends heavily on the intended production volume. Currently, most high volume designs are laid out manually and then digitized. Design rule verification programs are often used to validate adherence to the design constraints imposed by the technology. For custom design of low volume LSI circuits, automated layout packages such as PR2D and MP2D [5], LTX [6] and FAMOS [7] are often employed. The basic idea in these automatic approaches is to define cells such as logic gates and flipflops, and to place these in rows. The disadvantage of this row-based layout approach is that the silicon area required for the layout of a circuit is much larger than the area that can be obtained by means of a careful manual approach.

Recently, attempts have been made to partially automate the layout of high volume designs. An example of these attempts is the FLOSS system, developed at RCA [9]. An approach to less restrictive design of custom LSI circuits is currently being pursued by Sandia Laboratories with the SICLOPS system [8].

The main goals of the system that is being developed at Stanford are the following:

1. To provide a total design environment for integrated circuits, both high volume and low volume custom LSI circuits.

2. To allow the designer to choose between a purely manual approach, a totally automatic approach or any combination that best suits design cost/production trade-offs. In such an environment the designer could, e.g., make use of manual techniques to lay out basic functional blocks and then use an algorithmic approach to obtain a layout, which then could be further improved upon by manual editing.

3. In order to provide these characteristics, interactive graphics is an essential part of the design methodology.

4. To perform dynamic design rule verification. At any stage of the layout process, design rules will be checked. This will prevent a layout designer from making a serious mistake which may, in current systems, only be discovered much later.

5. Using the same philosophy, the system will dynamically check whether the structural properties, i.e., the connectivity of the circuit is violated.

6. The system will have the ability to functionally verify a part of the design, or the complete design, using circuit simulation or logic simulation, at any point in the design process.

7. The system will be as technologically-independent as possible. Design rules and other data relating to a specific technology

will be stored in a technology file.

2. THE OVER-ALL IC DESIGN SYSTEM

The over-all structure of the system is shown in Figure 1.

In order to explain the concepts involved in the system we will go through a simple design example; a 4-bit multiplier as shown in Figure 2.

The first phase in a design is to interactively specify the design. This is done by means of an interactive system that allows the designer to specify the structure of the system and of each of its subsystems at the various levels of abstraction defined by the designer.

An example of such an hierarchical specification is illustrated in Figure 2. At the highest level of abstraction the designer sees the 4-bit multiplier of Figure 2a as being constructed out of lower level primitives such as one-bit multipliers of type MULT1, NAND gates and inverters (Figure 2b). At the next level, the one-bit multiplier of type MULT1 is described in terms of flipflops of type DFF and a full adder of type FADD (Figure 2c).

At the following level both the flipflop of type DFF and the full adder of type FADD are described in terms of NAND gates and inverters, (Figure 2d, and Figure 2e). At the final level, the NAND gates and inverter are specified in terms of transistors using CMOS technology (Figure 2f, Figure 2g, Figure 2h, Figure 2i).

The structure of each of these interactively specified diagrams is translated into a language called SDL, the Structural Design Language [1]. The SDL specification corresponding to each of these diagrams is shown in Figure 3.

The designer will have at his disposition a macroexpansion capability which allows him to expand the total system, or a part of the system, to any level desired. The output of such an expansion is in the form of an intermediate language. By using an intermediate language expansion at the correct level the designer can perform a logic simulation at the flip-flop

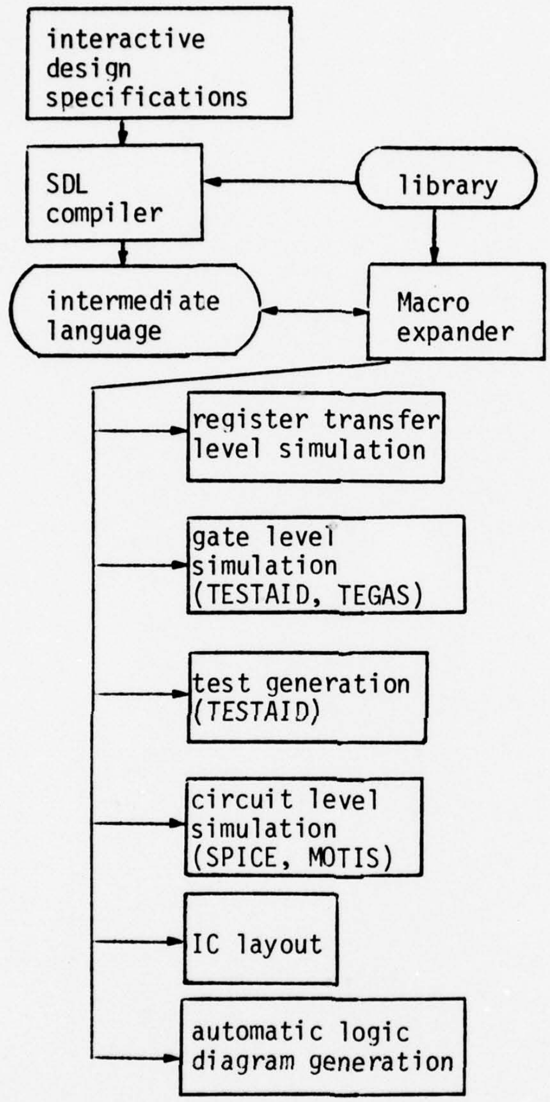


Figure 1: Structure of the IC design system

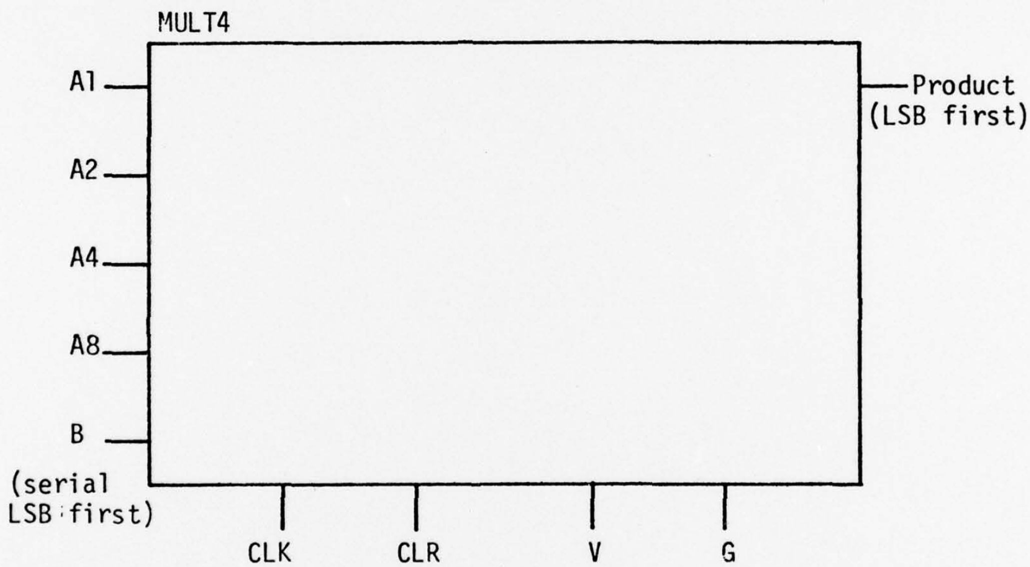


Figure 2a: 4-bit Multiplier MULT4

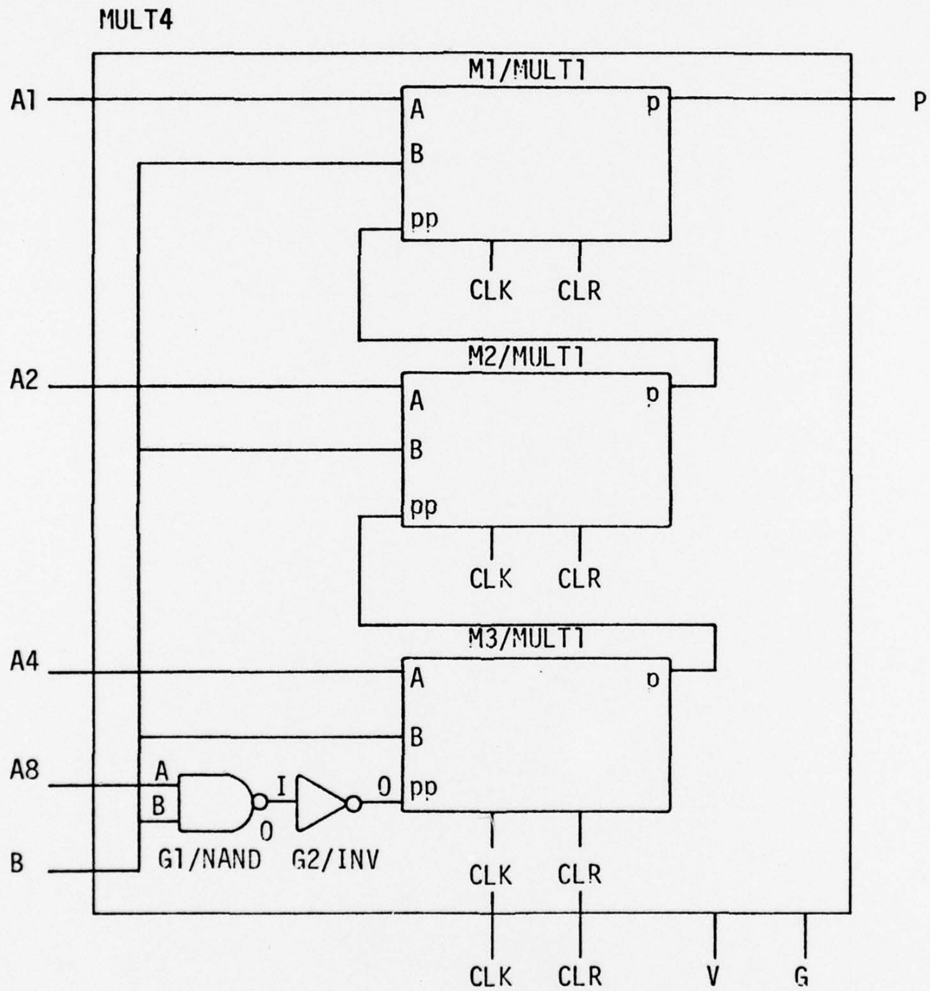


Figure 2b: Highest Level Description of MULT4 .

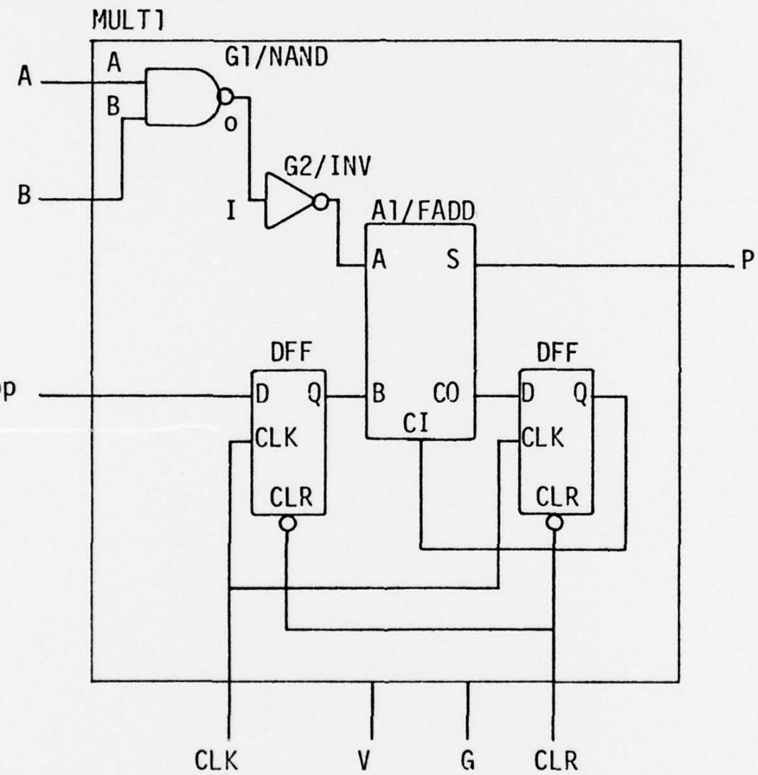


Figure 2c: One-bit Multiplier MULT1

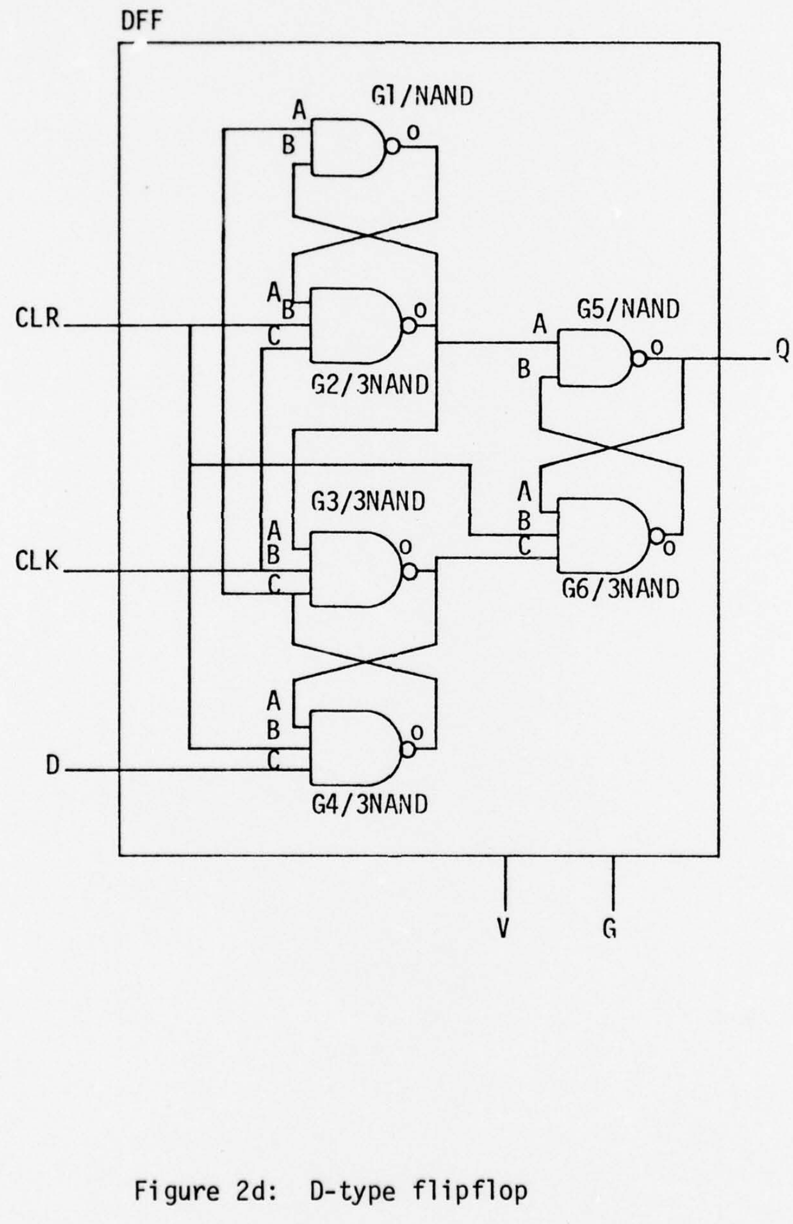


Figure 2d: D-type flipflop

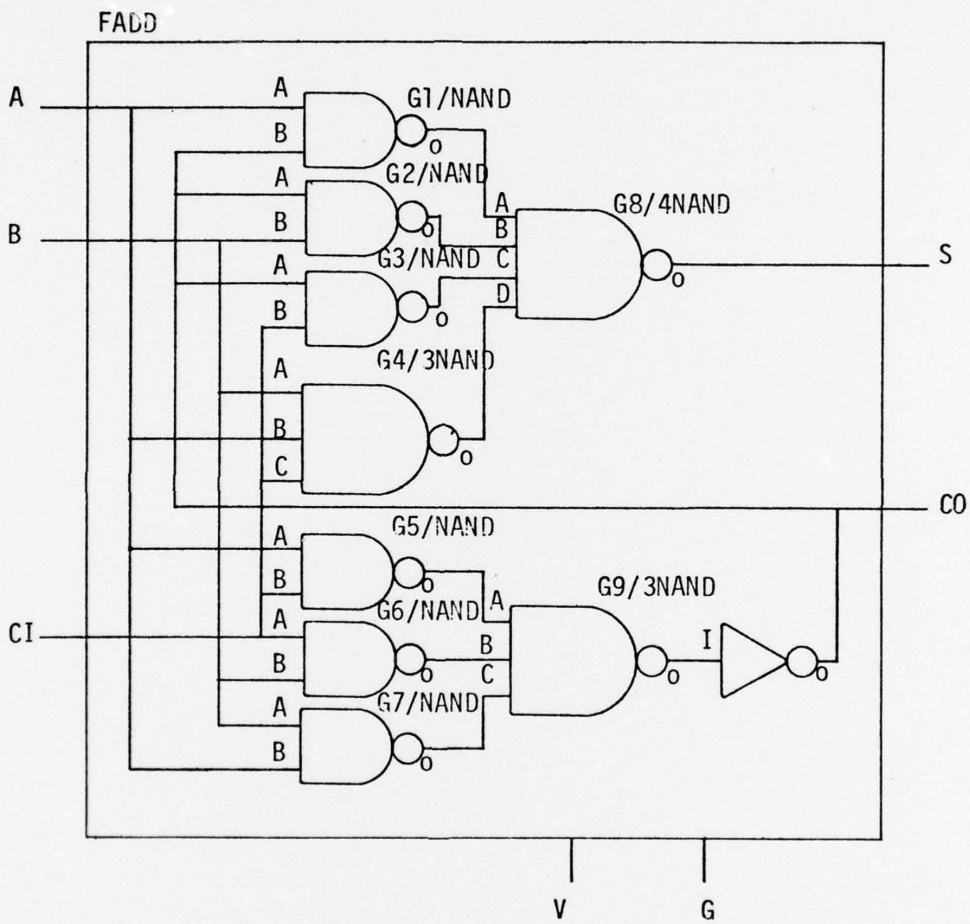


Figure 2e: Full Adder

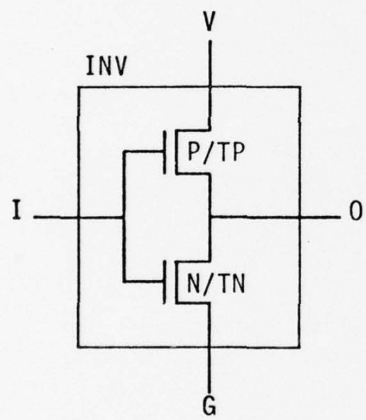


Figure 2f: CMOS Inverter

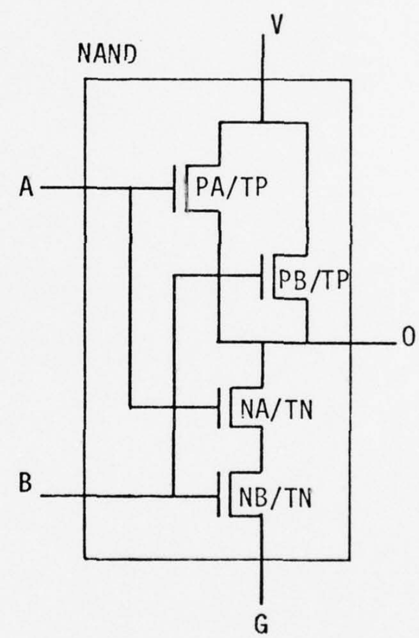


Figure 2g: CMOS 2-input NAND gate

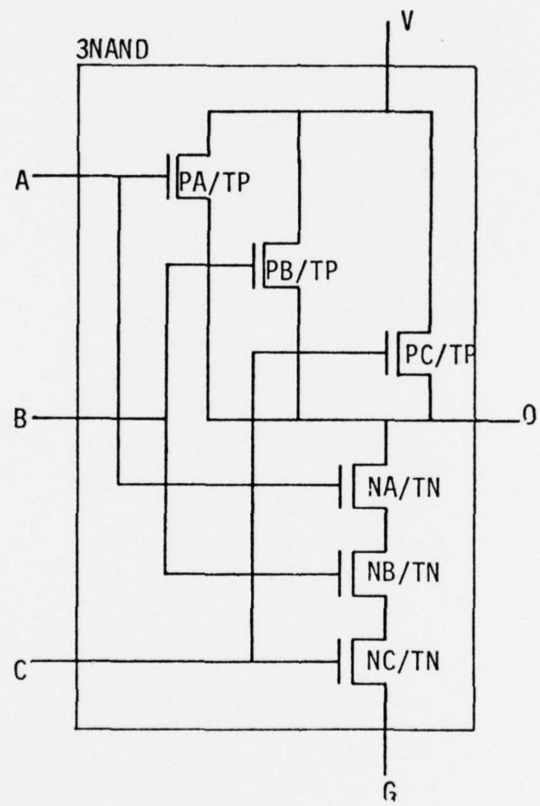


Figure 2h: CMOS 3-input NAND gate

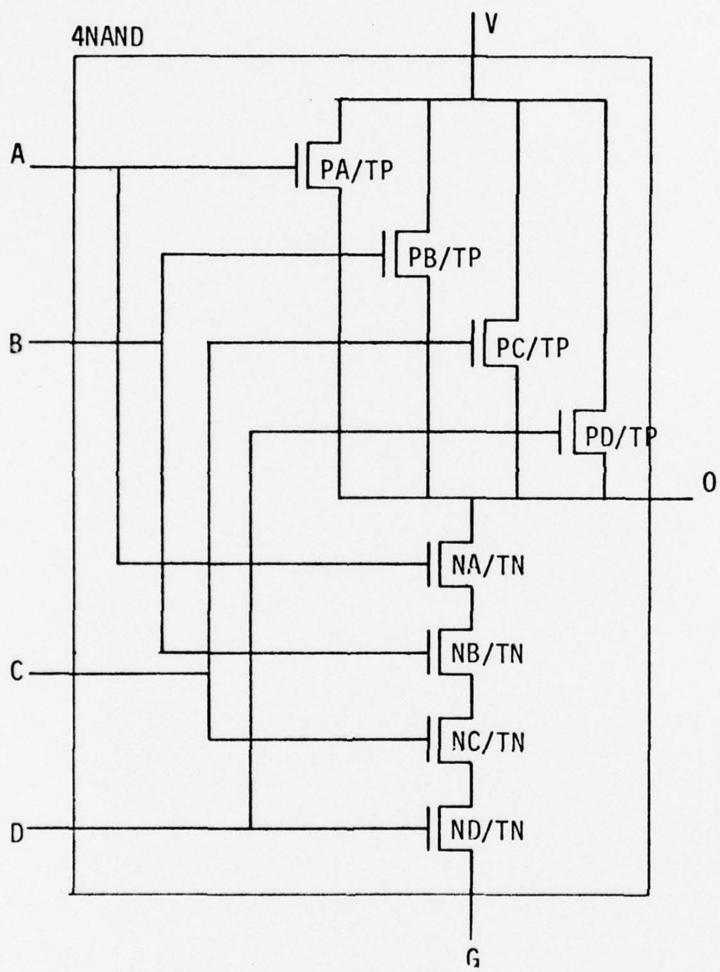


Figure 2i: CMOS 4-input NAND gate

```
USER:WMVC;
NAME:MULT4;
PURPOSE:ICDESIGN;
LEVEL:CHIP;
EXT::A1,A2,A4,A8,B,CLK,CLR,PRODUCT,V,GND;
INPUTS:A1,A2,A4,A8,B,CLK,CLR;
OUTPUTS:PRODUCT;
TYPES:MULT1,NAND,INV;
MULT1:M<1:3>;
INV:G2;
NAND:G1;
N1=.A1,M<1>.A;
N2=.A2,M<2>.A;
N3=.A4,M<3>.A;
N4=..A8,G1.A;
N5=.B,G1.B,M<1:3>.B;
N6=M<1>.P,.PRODUCT;
N7=.CLK,M<1:3>.CLK;
N8=.CLR,M<1:3>.CLR;
N9=M<1>.PP,M<2>.P;
N10=M<2>.PP,M<3>.P;
N11=G1.O,G2.I;
N12=G2.O,M3.PP;
END;
NAME:MULT1;
PURPOSE:ICDESIGN;
LEVEL:FF;
EXT::A,B,PP,CLK,CLR,P,V,GND;
INPUTS:A,B,PP,CLK,CLR;
OUTPUTS:PP;
TYPES:DFF,FADD,NAND,INV;
DFF:F1,F2;
FADD:A1;
NAND:G1;
INV:G2;
N1=.A,G1.A;
N2=.B,G1.B;
N3=.PP,F1.D;
N4=.CLK,F1.CK,F2.CK;
N5=.CLR,F1.CL,F2.CL;
N6=A1.S,.P;
N7=G1.O,G2.I;
N8=G2.O,A1.A;
N9=F1.Q,A1.B;
N10=A1.CO,F2.D;
N11=A1.CI,F2.Q;
END;
```

Figure 3: SDL representation of the design of Figure 2

```
NAME:DFF;
PURPOSE:ICDESIGN;
LEVEL:GATE;
EXT::CLK,CLR,D,Q,V,GND;
INPUTS:D,CLK,CLR;
OUTPUTS:Q;
TYPES:NAND,3NAND;
NAND:G1,G5;
3NAND:G2,G3,G4,G6;
N1=.CLR,G2.B,G4.B,G6.B;
N2=.CLK,G3.B,G2.C;
N3=.D,G4.C;
N4=G5.O,.Q,G6.A;
N5=G4.O,G3.C,G1.A;
N6=G3.O,G6.C,G4.A;
N7=G2.O,G5.A,G3.A,G1.B;
N8=G1.O,G2.A;
N9=G6.O,G5.B;
END;
NAME:FADD;
PURPOSE:ICDESIGN;
LEVEL:GATE;
EXT::A,B,CI,CO,S,V,GND;
INPUTS:A,B,CI;
OUTPUTS:CO,S;
TYPES:NAND,3NAND,4NAND,INV;
NAND:G1,G2,G3,G5,G6,G7;
3NAND:G4,G9;
4NAND:G8;
INV:G10;
N1=.A,G1.A,G4.B,G5.A,G7.B;
N2=.B,G2.B,G4.A,C6.B,G7.A;
N3=.CI,G6.A,G5.B,G4.C,G3.B;
N4=G1.O,G8.A;
N5=G2.O,G8.B;
N6=G3.O,G8.C;
N7=G4.O,G8.D;
N8=G5.O,G9.A;
N9=G6.O,G9.B;
N10=G7.O,G9.C;
N11=G8.O,.S;
N12=G9.O,G10.I;
N13=G10.O,G3.A,G1.B,G2.A,.CO;
END;
```

Figure 3: continued from preceding page

```
NAME:INV;
PURPOSE:ICDESIGN;
LEVEL:TRANS;
EXT::I,O,V,GND;
INPUTS:I;
OUTPUTS:O;
TYPES:TP,TN;
TN:NA;
TP:PA;
N1=.I,PA.G,NA.G;
N2=PA.D,NA.S,.O;
N3=.GND,NA.S;
N4=.V,PA.S;
END;
NAME:NAND;
PURPOSE:ICDESIGN;
LEVEL:TRANS;
EXT::A,B,O,V,GND;
INPUTS:A,B;
OUTPUTS:O;
TYPES:TP,TN;
TN:NA,NB;
TP:PA,PB;
N1=.A,PA.G,NA.G;
N2=PA.D,PB.D,NA.D,.O;
N3=.GND,NB.S;
N4=.V,PA.S,PB.S;
N5=.B,PB.G,NB.G;
N6=NA.S,NB.D;
END;
NAME:3NAND;
PURPOSE:ICDESIGN;
LEVEL:TRANS;
EXT::A,B,C,O,V,GND;
INPUTS:A,B,C;
OUTPUTS:O;
TYPES:TP,TN;
TN:NA,NB,NC;
TP:PA,PB,PC;
N1=.A,PA.G,NA.G;
N2=PA.D,PB.D,PC.D,NA.D,.O;
N3=.GND,NC.S;
N4=.V,PA.S,PB.S,PC.S;
N5=.B,PB.G,NB.G;
N6=NA.S,NB.D;
N7=.C,PC.G,NC.G;
N8=NB.S,NC.D;
END;
```

Figure 3: continued from preceding page

```
NAME:4NAND;
PURPOSE:ICDESIGN;
LEVEL:TRANS;
EXT::A,B,C,D,O,V,GND;
INPUTS:A,B,C,D;
OUTPUTS:O;
TYPES:TP,TN;
TN:NA,NB,NC,ND;
TP:PA,PB,PC,PD;
N1=.A,PA.G,NA.G;
N2=PA.D,PB.D,PC.D,PD.D,NA.D,.O;
N3=.GND,ND.S;
N4=.V,PA.S,PB.S,PC.S,PD.S;
N5=.B,PB.G,NB.G;
N6=NA.S,NB.D;
N7=.C,PC.G,NC.G;
N8=NB.S,NC.D;
N9=.D,PD.G,ND.G;
N10=NC.S,ND.D;
END;
NAME:TN;
PURPOSE:ICDESIGN;
LEVEL:END;
EXT::G,S,D;
END;
NAME:TP;
PURPOSE:ICDESIGN;
LEVEL:END;
EXT::G,D,S;
END;
CEND;
```

Figure 3: continued from preceding page

or gate level using, e.g., TESTAID [4] or a circuit simulation at the transistor level, using SPICE or MOTIS [2][3]. At the higher level, the designer could validate his design by means of a register-transfer-level simulation or functional simulation, if it were properly specified.

The hierarchical structure as specified by the logic designer constitutes a functional partitioning of the system. This information is conveyed to the layout subsystem which will also be hierarchical in nature. The layout subsystem will allow the designer to perform his task both in a top-down and a bottom-up fashion by making use of this functional partitioning information. The characteristics of the layout subsystem are, therefore, quite different from currently used systems such as Calma, Computervision and Applicon.

3. STRUCTURE OF THE IC LAYOUT SYSTEM

The layout system will be centered around a central design file which will contain all of the information relating to the design at any point in time. This file in itself will contain the hierarchical structure as derived from the functional partitioning presented by the logic designer. It will also contain any technological information necessary to accomplish a complete and correct layout. The structure of this system is shown in Figure 4.

The design file organization reflects the hierarchical nature of the design process, as it was specified by the designer. Figure 5 shows the storage structure associated with the 4-bit multiplier of Figure 2.

The highest level description of MULT4 points to the lower level description of MULT1, NAND and INV. In the design system only one block of the design will be in memory. The other blocks of the design will remain stored on a direct-access storage device. The transfer of control from one level of abstraction to another will be strictly under the control of the designer. The data structure for describing an object at a given level is illustrated in Figure 6.

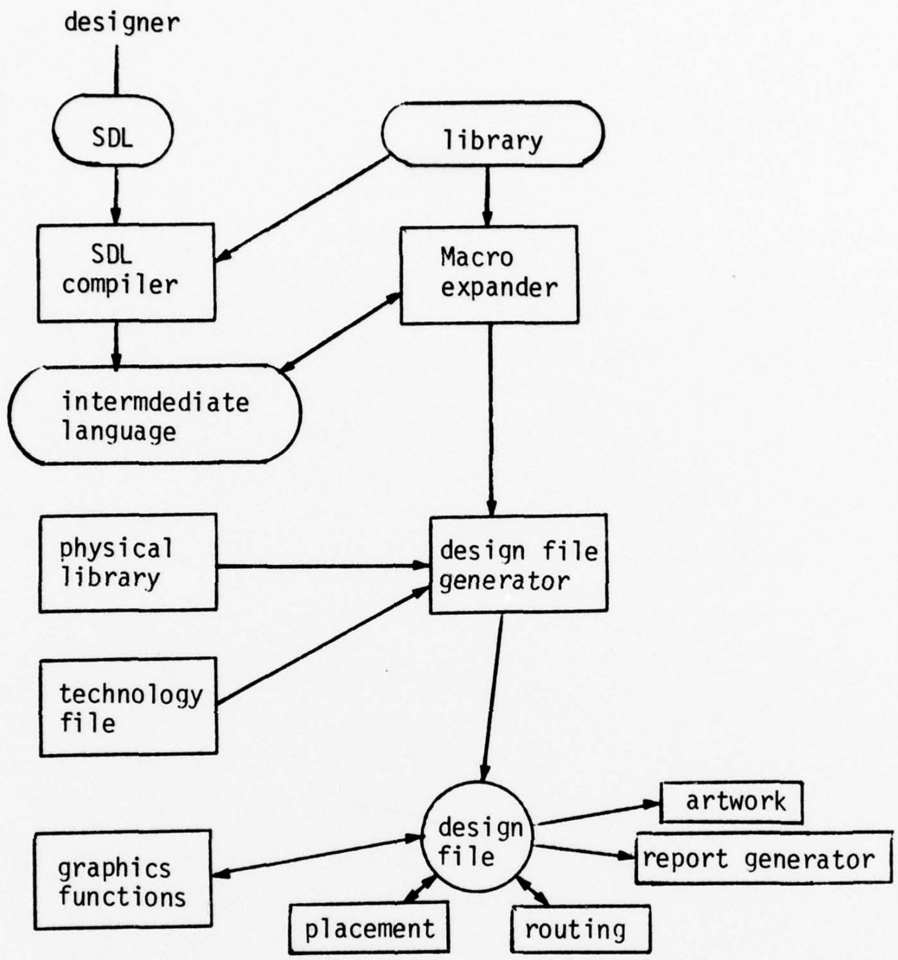


Figure 4: Structure of the IC layout system.

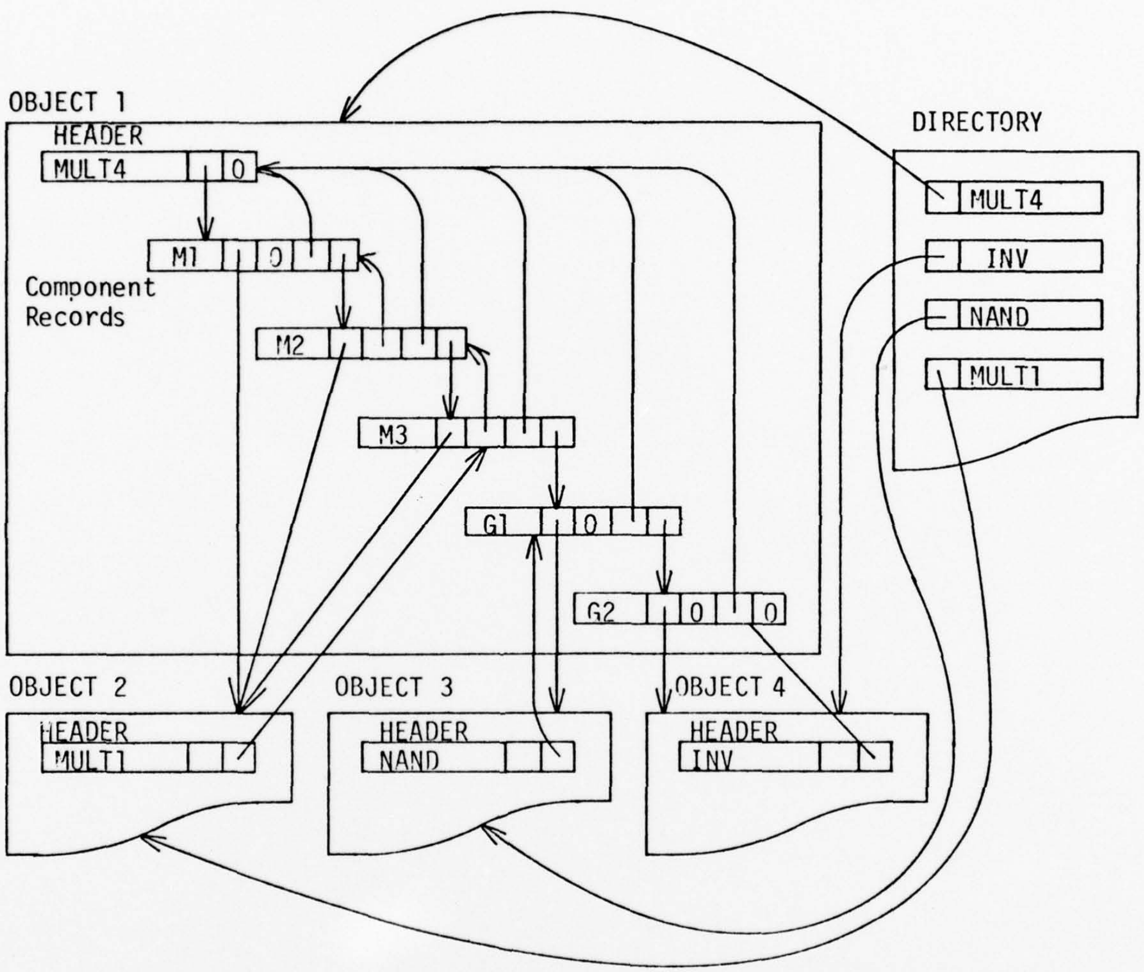


Figure 5: Hierarchical Structure of the Design File

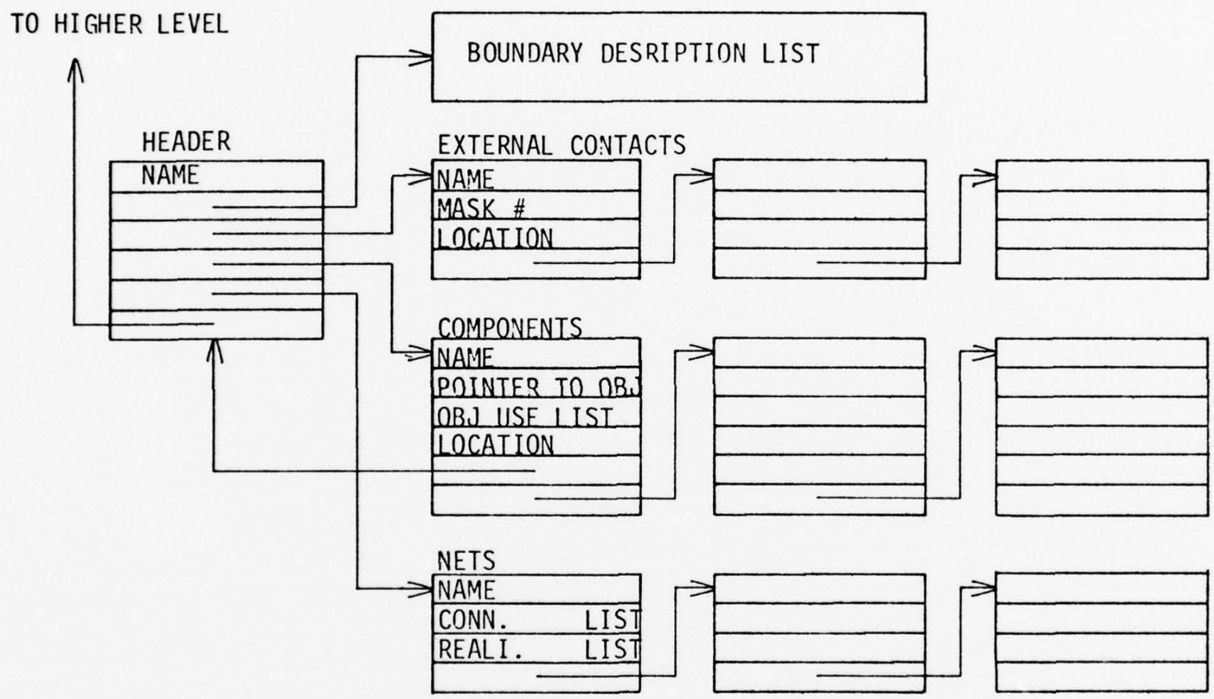


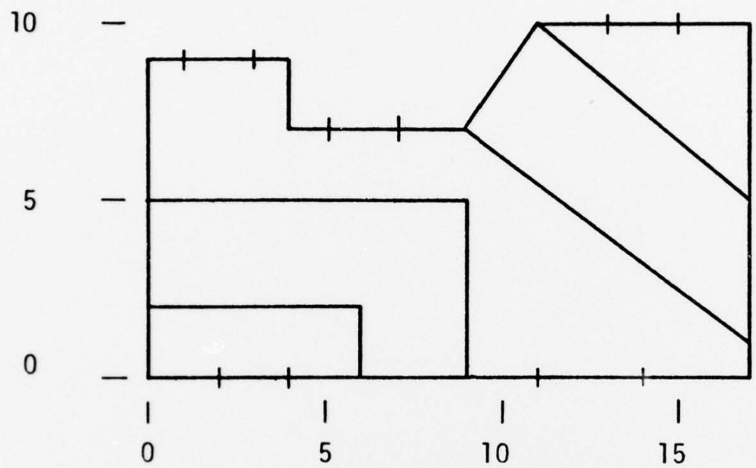
Figure 6: Object description data structure

This description contains information on the components used to construct this object, the signals that connect these components, the external contact points and the physical boundary description. The purpose of the boundary description is to specify the physical shape and size of the object. This is illustrated by the example in Figure 7. Besides the physical outline and the external contact locations the boundary description also describes the so-called exceptions, i.e., areas that can be used for routing of interconnections at a higher level.

The interactive graphics functions are characterized by the hierarchical nature of the system, i.e., they only work on one function block at a time. They will allow the designer to manually place and manipulate components, to manually route interconnections in addition to such standard features as zooming, panning, etc.

The initial implementation of the system will be oriented towards manual design techniques. Algorithms will then be implemented for placing components with arbitrary shapes and sizes and for routing the interconnections between them. It must be emphasized that these algorithms will operate at one level of the hierarchy only. In addition, topological layout methods based on previous work [10] will be incorporated into the system. Such methods would provide an initial topological design of a block. The final physical layout in such an approach would then be obtained using a physical area optimization technique similar to the one used in the FLOSS system [9]. Another algorithm will deal with estimating the area to be used by the design in order to allow the designer to determine optimal shapes of cells.

A further feature that is currently being planned is to allow the user to interactively specify a subcircuit of the total design. This subcircuit would then be output in SDL. It will be possible for the designer to perform a gate-level logic simulation on this subcircuit by means of TESTAID [2] or circuit simulation by means of MOTIS [3] or SPICE [2]. After a macro-expansion to the appropriate level this subcircuit could then be laid out by




```
BOUNDARY:    0.0,17.0,17.11,11.11,9.7,4.7,4.9,0.9,0.0;

EXCEPTIONS:  LEVEL=METAL,0.2,6.2,6.0,9.0,9.5,0.5,0.2/
                         9.7,17.1,17.5,11.11,9.7;

CONNECTORS:  LEVEL=METAL,(1.9,3.9)(5.7,7.7),(11.0,14.0),
             LEVEL=POLYSI,(2.0,4.0),(13.10,15.10);
```

Figure 7: Example of a Physical Boundary Description

means of an automated layout system such as SICLOPS [8].

4. FUNCTIONAL CHARACTERISTICS OF THE IC LAYOUT SYSTEM

The design process starts with the specification of the logical aspects of the design. This can either be done with the interactive logic diagram drawing subsystem or by encoding the design directly in SDL. The design is then compiled and expanded by the SDL subsystem. The designer at this point chooses at what level the SDL expansion terminates. If a low level is chosen, i.e., transistors, then only this level and any lower are fetched from the physical library. If, however, a higher level such as gate or register is selected, more information is fetched from the library. If the designer desires quick turn around, automatic or semi-automatic, he would choose to limit the amount of expansion at the SDL stage and use the standard layouts that are in the library. On the other hand, if the design is for high volume production and a hand-tuned layout is needed, then the designer has the SDL subsystem expand the circuit to the lowest level. While interactive layout is taking place the designer can fetch any blocks that are in the library and include them in his layout.

The basic idea in the layout subsystem is that the designer only works at one level of abstraction at a time. This means that he can only place components that are defined at that level. For instance, at a given level the designer would be able to place cells representing flip-flops and to route interconnections between these cells. He would, however, not be able to change the shape of a cell if that would result in a denser packaging. In order to do that, he would have to go to a lower level and rearrange the components at that level in order to obtain a more favorable shape for the cell design.

Typically, the manual layout of an IC would consist of two phases. The first phase being the preliminary design phase consisting of the following steps:

1. Estimate the size of components at every level by using information

from the library about the components at the lowest level.

2. Perform an initial placement, either manually or automatically.
3. Determine the shapes of the components at this level for dense packing.
4. Go to the next level and repeat steps 2, and 3 for each component at this level.
5. Reiterate this process for the next levels of abstraction.
6. Go back to the highest level and step 1 to reiterate the process. This first phase of the design would provide the designer with a reasonably accurate estimate of the shapes and sizes of all of the components at the various levels. The final layout, though, would have to be performed bottom-up using the information obtained in the first phase.

The second phase is really the detailed final design and is performed in a bottom-up fashion. It consists of the following steps:

1. Using the cells at the lowest level, design components at the next lowest level. This gives the shapes and sizes of the components at that level.
2. Repeat this process for the next lowest level and so on, until finally the layout is performed for the complete chip.
3. If the total layout is not satisfactory, one can go back and change the cell shape at the lower level and then from there on repeat the process.

If the designer does not want to do a cell shape and placement estimate he can skip phase 1 and go directly to phase 2. Phase 1 can also be done partially and at any time so the designer can use any mixture of phase 1 and 2 that he finds most useful.

As an example, take the 4-bit multiplier described earlier, MULT4. To layout this circuit the designer would first use the interactive logic drawing subsystem to draw the overall outline and the external connections (Figure 2a). He would then specify what MULT4 is constructed of by filling in the next level down (Figure 2b). He would then specify in a new drawing the construction of each of the components that were used to construct MULT4. There are three types of components used: MULT1, NAND, INV. MULT1 is specified next (Figure 2c). The specification of NAND and INV are postponed since they belong to a lower level than MULT1. The next step is to repeat the process of specifying the components of the objects already defined until the desired level of detail is reached. The example has been specified down to transistors. MULT1 has 4 types of components, FADD, DFF, NAND, INV. The full adder and the D flipflop are described in terms of gates (Figure 2d and 2e). On the next level are the descriptions of the gates INV, NAND, 3NAND, 4NAND in terms of transistors (Figure 2f, 2g, 2h, 2i). The example is described in CMOS technology. The lowest level of description is that of the transistors themselves. There are two types of transistors used in the example: n-channel and p-channel.

The description of MULT4 would only be carried down to this level of detail if the designer were interested in a manual design. If the designer desired an automatic design he would have left the description in terms of higher-level components.

The information in the drawings is now converted to SDL format and fed to the SDL compiler. The output of the compiler is then loaded into a design file and the interactive layout of the circuit is started.

The system will first estimate the size of the cells at every level. The designer then starts at the MULT4 level and with the aid of the system places the 3 instances of MULT1, the NAND and the INV and determines their shapes. He then repeats this process at each lower level until the transistor level is reaches.

The next step is the actual layout of the chip. The transistor shapes were fetched from the physical library. The designer interactively combines the transistors to form the gates. The gates are then used to build the DFF and the FADD. These two are used to construct MULT1, and finally, MULT4 is constructed.

5. CURRENT STATUS

The SDL compiler and expansion facility is currently operational. An interface from SDL to the Hewlett-Packard Testaid system has been implemented, giving a logic simulation and test generation capability. Furthermore, an automated logic diagram generation system that produces logic diagrams from and SDL description has been implemented [11].

The interactive design specification subsystem will be operational by late 1977. The nucleus of the IC layout subsystem, i.e., the design file access functions and the primitive graphics functions are scheduled for completion by the first quarter of 1978. At that time, an interface to SPICE and MOTIS will also become available. The algorithmic functions of the system will be implemented following this.

Currently, most of the software runs on an IBM 370/168 system and makes use of a Tektronix 4013 storage tube terminal. It is the intention to transfer the system to a large 32-bit minicomputer with extensive color-graphics facilities.

Acknowledgements

The authors would like to thank Willis Marti, Jon Hupp, Peter Chang and Bryan Preas for their valuable comments.

They are greatly indebted to Marlene Rothstein for typing several versions of the manuscript.

REFERENCES

[1] vanCleemput, W. M., "A Hierarchical Language for the Structural Description of Digital Systems," Proc. 14th Design Automation Conference, New Orleans, La., June 1977, pp. 378-385.

[2] Nagel, L. W. and D. O. Pederson, "SPICE," University of California, Berkeley, Electronics Research Laboratory, Technical Report, April, 1973.

[3] Chawla, B. R., H. K. Gummel and P. Kozak, "MOTIS - An MOS Timing Simulator," IEEE Trans. Circuits and Systems, Vol. CAS-22, no. 12, pp. 901-919, December 1975.

[4] Hewlett-Packard Co., Testaid III, Programming and Operating Manual, Publication No. 91075-93008, November 1976.

[5] Feller, A., "Automatic Layout of Low-Cost Quick-Turnaround Random Logic Custom LSI Devices," Proc. 13th Design Automation Conference, San Francisco, Ca., June 1976, pp. 79-85.

[6] Deutsch, D. N., G. Persky and D. G. Schweikert, "LTX, A System for the Directed Automatic Design of LSI Circuits," Proc. 13th Design Automation Conference, San Francisco, Ca., June 1976, pp. 399-607.

[7] Mattison, R. L., "A High Quality Low-Cost Router for MOS/LSI," Proc. 9th Design Automation Workshop, Dallas, Texas, June 1972, pp. 94-103.

[8] Preas, B. T. and C. Gwynn, "Architecture for Contemporary Computer Aids to Generate IC Mask Layouts," Proc. 11th Asilomar Conference on Circuits, System, Computers, Pacific Grove., Ca., November 1977.

[9] Cho, Y. E., A. J. Korenjak and D. E. Stockton, "FLOSS: An Approach to Automated Layout for High-Volume Designs," Proc. 14th Design Automation Conference, New Orleans, La., June 1977, pp. 138-141.

[10] vanCleemput, W. M., "Mathematical Models for the Circuit Layout Problem," IEEE Trans. on Circuits and Systems, Vol. 23, No. 12, December 1976, pp. 759-767.

[11] Smith, J. A. and J. G. Linders, "Automatic Generation of Logic Diagrams," Proc. 13th Design Automation Conference, San Francisco, Ca., June 1976, pp. 377-391.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER
Technical Note # 132

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)
Initial Design Considerations for a Hierarchical IC Design System

5. TYPE OF REPORT & PERIOD COVERED
Technical Note

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
W. M. vanCleemput & E. A. Slutz

8. CONTRACT OR GRANT NUMBER(s)
N-00014-75-C-0601

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Stanford Electronics Laboratories
Stanford University
Stanford, CA 94305

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

11. CONTROLLING OFFICE NAME AND ADDRESS
Office of the Naval Research
Department of the Navy
Washington, DC 22217

12. REPORT DATE
November 1977

13. NO. OF PAGES
27

14. MONITORING AGENCY NAME & ADDRESS (if diff. from Controlling Office)

15. SECURITY CLASS. (of this report)
unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this report)
Reproduction in whole or part in permitted for any purpose of the United States Government.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
integrated circuit design, hierarchical design system, design automation, LSI circuit layout

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
This paper describes the initial design of a comprehensive hierarchical integrated circuit design system, that is currently being implemented at Stanford University. This system encourages the use of structured hardware design techniques. It is intended for the design and layout of large-scale integrated circuits by means of a combination of manual and algorithmic techniques.

DD FORM 1 JAN 73 1473
EDITION OF 1 NOV 65 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

JSEP REPORTS DISTRIBUTION LIST

Department of Defense

Director
National Security Agency
Attn: Dr. T. J. Beahn
Fort George G. Meade, MD 20755

Defense Documentation Center (12)
Attn: DDC-TCA (Mrs. V. Caponio)
Cameron Station
Alexandria, VA 22314

Assistant Director
Electronics and Computer Sciences
Office of Director of Defense
Research and Engineering
The Pentagon
Washington, D.C. 20315

Defense Advanced Research
Projects Agency
Attn: (Dr. R. Reynolds)
1400 Wilson Boulevard
Arlington, VA 22209

Department of the Army

Commandant
US Army Air Defense School
Attn: ATSAD-T-CSM
Fort Bliss, TX 79916

Commander
US Army Armament R&D Command
Attn: DRSAR-RD
Dover, NJ 07801

Commander
US Army Ballistics Research Lab.
Attn: DRXRD-BAD
Aberdeen Proving Ground
Aberdeen, MD 21005

Commandant
US Army Command and
General Staff College
Attn: Acquisitions, Library Div.
Fort Leavenworth, KS 66027

Commander
US Army Communication Command
Attn: CC-OPS-PD
Fort Huachuca, AZ 85613

Commander
US Army Materials and
Mechanics Research Center
Attn: Chief, Materials Sci. Div.
Watertown, MA 02172

Commander
US Army Materiel Development
and Readiness Command
Attn: Technical Lib., Rm. 7S 35
5001 Eisenhower Avenue
Alexandria, VA 22333

Commander
US Army Missile R&D Command
Attn: Chief, Document Section
Redstone Arsenal, AL 35809

Commander
US Army Satellite Communications
Agency
Fort Monmouth, NJ 07703

Director
US Army Signals Warfare Laboratory
Attn: DELSW-OS
Arlington Hall Station
Arlington, VA 22212

Project Manager
ARTADS
EAI Building
West Long Branch, NJ 07764

NOTE: One (1) copy to each addressee unless otherwise indicated.

Commander/Director
Atmospheric Sciences Lab. (ECOM)
Attn: DRSEL-BL-DD
White Sands Missile Range, NM 88002

Commander
US Army Electronics Command
Attn: DRSEL-NL-O
(Dr. H. S. Bennett)
Fort Monmouth, NJ 07703

Director
TRI-TAC
Attn: TT-AD (Mrs. Briller)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-CT-L (Dr. R. Buser)
Fort Monmouth, NJ 07703

Director
Electronic Warfare Lab. (ECOM)
Attn: DRSEL-WL-MY
White Sands Missile Range, NM 88002

Executive Secretary, TAC/JSEP
US Army Research Office
P. O. Box 12211
Research Triangle Park, NC 27709

Commander
Frankford Arsenal
Deputy Director
Pitman-Dunn Laboratory
Philadelphia, PA 19137

Project Manager
Ballistic Missile Defense
Program Office
Attn: DACS-DMP (Mr. A. Gold)
1300 Wilson Boulevard
Arlington, VA 22209

Commander
Harry Diamond Laboratories
Attn: Mr. John E. Rosenberg
2800 Powder Mill Road
Adelphi, MD 20783

HQDA (DAMA-ARZ-A)
Washington, D.C. 20310

Commander
US Army Electronics Command
Attn: DRSEL-TL-E (Dr. J. A. Kohn)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-TL-EN
(Dr. S. Kroenenberg)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-NL-T (Mr. R. Kulinyi)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-NL-B (Dr. E. Lieblein)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-TL-MM (Mr. N. Lipetz)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-RD-O (Dr. W. S. McAfee)
Fort Monmouth, NJ 07703

Director
Night Vision Laboratory
Attn: DRSEL-NV-D
Fort Belvoir, VA 22060

Col. Robert Noce
Senior Standardization Representative
US Army Standardization Group, Canada
Canadian Force Headquarters
Ottawa, Ontario, Canada KIA)K2

Commander
US Army Electronics Command
Attn: DRSEL-NL-B (Dr. D. C. Pearce)
Fort Monmouth, NJ 07703

Commander
Picatinny Arsenal
Attn: SMUPA-TS-T-S
Dover, NJ 07801

Commander
US Army Electronics Command
Attn: DRSEL-NL-RH-1
(Dr. F. Schwering)
Fort Monmouth, NJ 07703

Commander
US Army Electronics Command
Attn: DRSEL-TL-I
(Dr. C. G. Thornton)
Fort Monmouth, NJ 07703

US Army Research Office (3)
Attn: Library
P. O. Box 12211
Research Triangle Park, NC 27709

Director
Division of Neuropsychiatry
Walter Reed Army Institute
of Research
Washington, D.C. 20012

Commander
White Sands Missile Range
Attn: STEWS-ID-R
White Sands Missile Range, NM 88002

Department of the Air Force

Mr. Robert Barrett
RADC/ETS
Hanscom AFB, MA 01731

Dr. Carl E. Baum
AFWL (ES)
Kirtland AFB, NM 87117

Dr. E. Champagne
AFAL/DH
Wright-Patterson AFB, OH 45433

Dr. R. P. Dolan
RADC/ETSD
Hanscom AFB, MA 01731

Mr. W. Edwards
AFAL/TE
Wright-Patterson AFB, OH 45433

Professor R. E. Fontana
Head, Dept. of Electrical Engineering
AFIT/ENE
Wright-Patterson AFB, OH 45433

Dr. Alan Garscadden
AFAPL/POD
Wright-Patterson AFB, OH 45433

USAF European Office of
Aerospace Research
Attn: Major J. Gorrell
Box 14, FPO, New York 09510

LTC Richard J. Gowen
Department of Electrical Engineering
USAF Academy, CO 80840

Mr. Murray Kesselman (ISCA)
Rome Air Development Center
Griffiss AFB, NY 13441

Dr. G. Knausenberger
Air Force Member, TAC
Air Force Office of Scientific
Research, (AFSC) AFSOR/NE
Bolling Air Force Base, DC 20332

Dr. L. Kravitz
Air Force Member, TAC
Air Force Office of Scientific
Research, (AFSC) AFSOR/NE
Bolling Air Force Base, DC 20332

Mr. R. D. Larson
AFAL/DHR
Wright-Patterson AFB, OH 45433

Dr. Richard B. Mack
RADC/ETER
Hanscom AFB, MA 01731

Mr. John Mottsmith (MCIT)
HQ ESD (AFSC)
Hanscom AFB, MA 01731

Dr. Richard Picard
RADC/ETSL
Hanscom AFB, MA 01731

Dr. J. Ryles
Chief Scientist
AFAL/CA
Wright-Patterson AFB, OH 45433

Dr. Allan Schell
RADC/ETE
Hanscom AFB, MA 01731

Mr. H. E. Webb, Jr. (ISCP)
Rome Air Development Center
Griffiss AFB, NY 13441

LTC G. Wepfer
Air Force Office of Scientific
Research, (AFSC) AFOSR/NP
Bolling Air Force Base, DC 20332

LTC G. McKemie
Air Force Office of Scientific
Research, (AFSC) AFOSR/NM
Bolling Air Force Base, DC 20332

Department of the Navy

Dr. R. S. Allgaier
Naval Surface Weapons Center
Code WR-303
White Oak
Silver Spring, MD 20910

Naval Weapons Center
Attn: Code 5515, H. F. Blazek
China Lake, CA 93555

Dr. H. L. Blood
Technical Director
Naval Undersea Center
San Diego, CA 95152

Naval Research Laboratory
Attn: Code 5200, A. Brodzinsky
4555 Overlook Avenue, SW
Washington, D.C. 20375

Naval Research Laboratory
Attn: Code 7701, J. D. Brown
4555 Overlook Avenue, SW
Washington, D.C. 20375

Naval Research Laboratory
Attn: Code 5210, J. E. Davey
4555 Overlook Avenue, SW
Washington, D.C. 20375

Naval Research Laboratory
Attn: Code 5460/5410, J. R. Davis
4555 Overlook Avenue, SW
Washington, D.C. 20375

Naval Ocean Systems Center
Attn: Code 75, W. J. Dejka
271 Catalina Boulevard
San Diego, CA 92152

Naval Weapons Center
Attn: Code 601, F. C. Essig
China Lake, CA 93555

Naval Research Laboratory
Attn: Code 5510, W. L. Faust
4555 Overlook Avenue, SW
Washington, D.C. 20375

Naval Research Laboratory
Attn: Code 2627, Mrs. D. Folen
4555 Overlook Avenue, SW
Washington, D.C. 20375

Dr. Robert R. Fossum
Dean of Research
Naval Postgraduate School
Monterey, CA 93940

Dr. G. G. Gould
Technical Director
Naval Coastal System Laboratory
Panama City, FL 32401

Naval Ocean Systems Center
Attn: Code 7203, V. E. Hildebrand
271 Catalina Boulevard
San Diego, CA 92152

Naval Ocean Systems Center
Attn: Code 753, P. H. Johnson
271 Catalina Boulevard
San Diego, CA 92152

Donald E. Kirk
Professor and Chairman
Electronic Engineer, SP-304
Naval Postgraduate School
Monterey, CA 93940

Naval Air Development Center
Attn: Code 01, Dr. R. K. Lobb
Johnsville
Warminster, PA 18974

Naval Research Laboratory
Attn: Code 5270, B. D. McCombe
4555 Overlook Avenue, SW
Washington, D.C. 20375

Capt. R. B. Meeks
Naval Sea Systems Command
NC #3
2531 Jefferson Davis Highway
Arlington, VA 20362

Dr. H. J. Mueller
Naval Air Systems Command
Code 310
JP #1
1411 Jefferson Davis Highway
Arlington, VA 20360

Dr. J. H. Mills, Jr.
Naval Surface Weapons Center
Electronics Systems Department
Code DF
Dahlgren, VA 22448

Naval Ocean Systems Center
Attn: Code 702, H. T. Mortimer
271 Catalina Boulevard
San Diego, CA 92152

Naval Air Development Center
Attn: Technical Library
Johnsville
Warminster, PA 18974

Naval Ocean Systems Center
Attn: Technical Library
271 Catalina Boulevard
San Diego, CA 92152

Naval Research Laboratory
Underwater Sound Reference Division
Technical Library
P. O. Box 8337
Orlando, FL 32806

Naval Surface Weapons Center
Attn: Technical Library
Code DX-21
Dahlgren, VA 22448

Naval Surface Weapons Center
Attn: Technical Library
Building 1-330, Code WX-40
White Oak
Silver Spring, MD 20910

Naval Training Equipment Center
Attn: Technical Library
Orlando, FL 32813

Naval Undersea Center
Attn: Technical Library
San Diego, CA 92152

Naval Underwater Systems Center
Attn: Technical Library
Newport, RI 02840

Office of Naval Research
Electronic and Solid State
Sciences Program (Code 427)
800 North Quincy Street
Arlington, VA 22217

Office of Naval Research
Mathematics Program (Code 432)
800 North Quincy Street
Arlington, VA 22217

Office of Naval Research
Naval Systems Division
Code 220/221
800 North Quincy Street
Arlington, VA 22217

Director
Office of Naval Research
New York Area Office
715 Broadway, 5th Floor
New York, NY 10003

Office of Naval Research
San Francisco Area Office
One Hallidie Plaza, Suite 601
San Francisco, CA 94102

Director
Office of Naval Research
Branch Office
495 Summer Street
Boston, MA 02210

Director
Office of Naval Research
Branch Office
536 South Clark Street
Chicago, IL 60605

Director
Office of Naval Research
Branch Office
1030 East Green Street
Pasadena, CA 91101

Mr. H. R. Riedl
Naval Surface Weapons Center
Code WR-34
White Oak Laboratory
Silver Spring, MD 20910

Naval Air Development Center
Attn: Code 202, T. J. Shopple
Johnsville
Warminster, PA 18974

Naval Research Laboratory
Attn: Code 5403, J. E. Shore
4555 Overlook Avenue, SW
Washington, D.C. 20375

A. L. Slafkovsky
Scientific Advisor
Headquarters Marine Corps
MC-RD-1
Arlington Annex
Washington, D.C. 20380

Harris B. Stone
Office of Research, Development,
Test and Evaluation
NOP-987
The Pentagon, Room 5D760
Washington, D.C. 20350

Mr. L. Sumney
Naval Electronics Systems Command
Code 3042, NC #1
2511 Jefferson Davis Highway
Arlington, VA 20360

David W. Taylor
Naval Ship Research and
Development Center
Code 522.1
Bethesda, MD 20084

Naval Research Laboratory
Attn: Code 4105, Dr. S. Teitler
4555 Overlook Avenue, SW
Washington, D.C. 20375

Lt. Cdr. John Turner
NAVMAT 0343
CP #5, Room 1044
2211 Jefferson Davis Highway
Arlington, VA 20360

Naval Ocean Systems Center
Attn: Code 746, H. H. Wieder
271 Catalina Boulevard
San Diego, CA 92152

Dr. W. A. Von Winkle
Associate Technical Director
for Technology
Naval Underwater Systems Center
New London, CT 06320

Dr. Gernot M. R. Winkler
Director, Time Service
US Naval Observatory
Massachusetts Avenue at
34th Street, NW
Washington, D.C. 20390

<u>Other Government Agencies</u>

Dr. Howard W. Etzel
Deputy Director
Division of Materials Research
National Science Foundation
1800 G Street
Washington, D.C. 20550

Mr. J. C. French
National Bureau of Standards
Electronics Technology Division
Washington, D.C. 20234

Dr. Jay Harris
Program Director
Devices and Waves Program
National Science Foundation
1800 G Street
Washington, D.C. 20550

Los Alamos Scientific Laboratory
Attn: Reports Library
P. O. Box 1663
Los Alamos, NM 87544

Dr. Dean Mitchell
Program Director
Solid-State Physics
Division of Materials Research
National Science Foundation
1800 G Street
Washington, D.C. 20550

Mr. F. C. Schwenk, RD-T
National Aeronautics and
Space Administration
Washington, D.C. 20546

M. Zane Thornton
Deputy Director, Institute for
Computer Sciences and Technology
National Bureau of Standards
Washington, D.C. 20234

Nongovernment Agencies

Director
Columbia Radiation Laboratory
Columbia University
538 West 120th Street
New York, NY 10027

Director
Coordinated Science Laboratory
University of Illinois
Urbana, IL 61801

Director of Laboratories
Division of Engineering and
Applied Physics
Harvard University
Pierce Hall
Cambridge, MA 02138

Director
Electronics Research Center
The University of Texas
Engineering-Science Bldg. 112
Austin, TX 78712

Director
Electronics Research Laboratory
University of California
Berkeley, CA 94720

Director
Electronics Sciences Laboratory
University of Southern California
Los Angeles, CA 90007

Director
Microwave Research Institute
Polytechnic Institute of New York
333 Jay Street
Brooklyn, NY 11201

Director
Research Laboratory of Electronics
Massachusetts Institute of Technology
Cambridge, MA 02139

Director
Stanford Electronics Laboratory
Stanford University
Stanford, CA 94305

Stanford Ginzton Laboratory
Stanford University
Stanford, CA 94305

Officer in Charge
Carderock Laboratory
Code 18 - G. H. Gleissner
David Taylor Naval Ship Research
and Development Center
Bethesda, MD 20084

Dr. Roy F. Potter
3868 Talbot Street
San Diego, CA 92106